

FIG 2

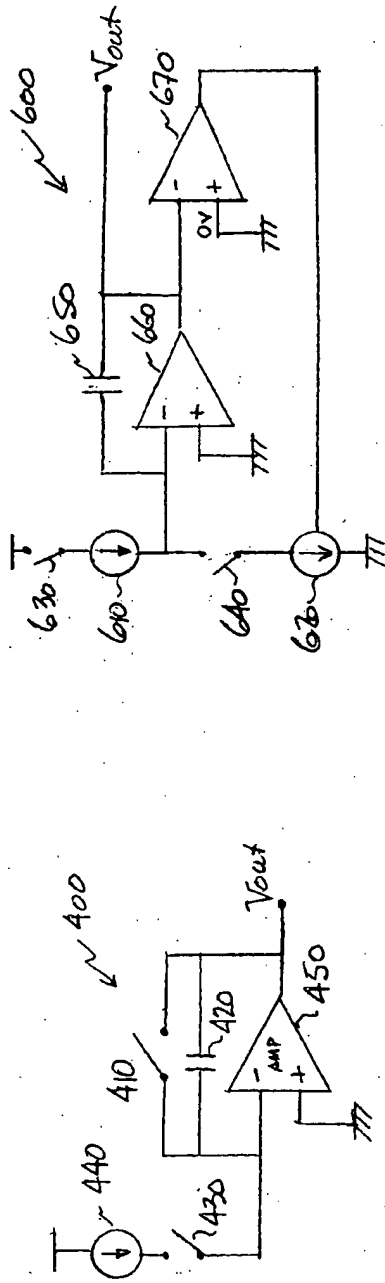


FIG 4

FIG 6

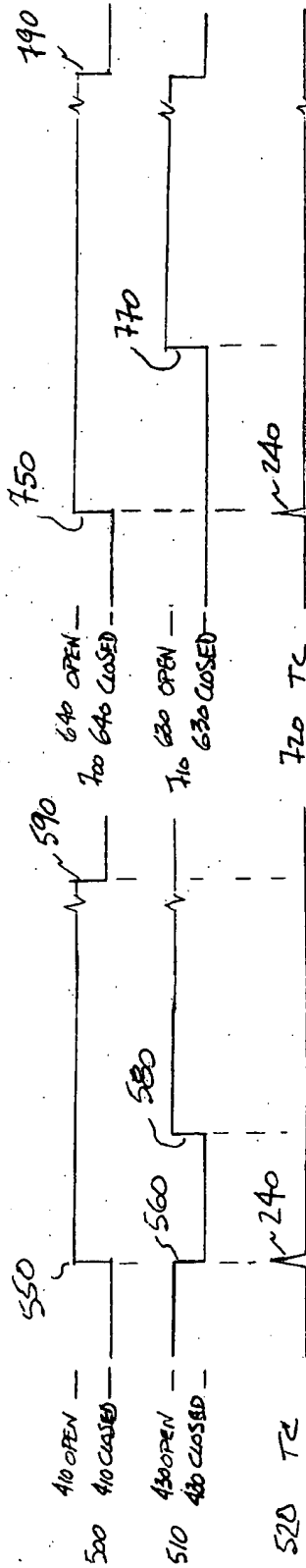
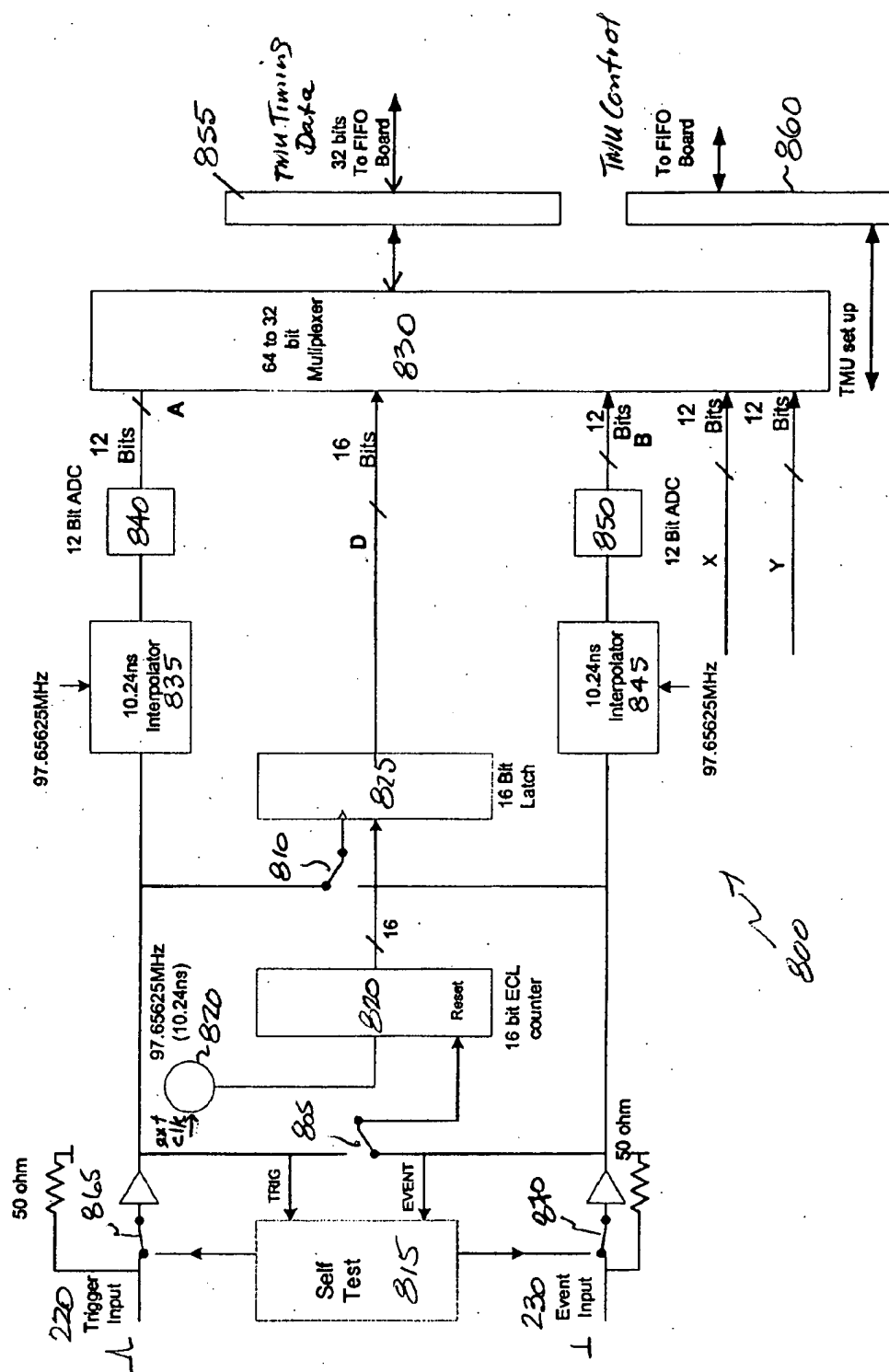
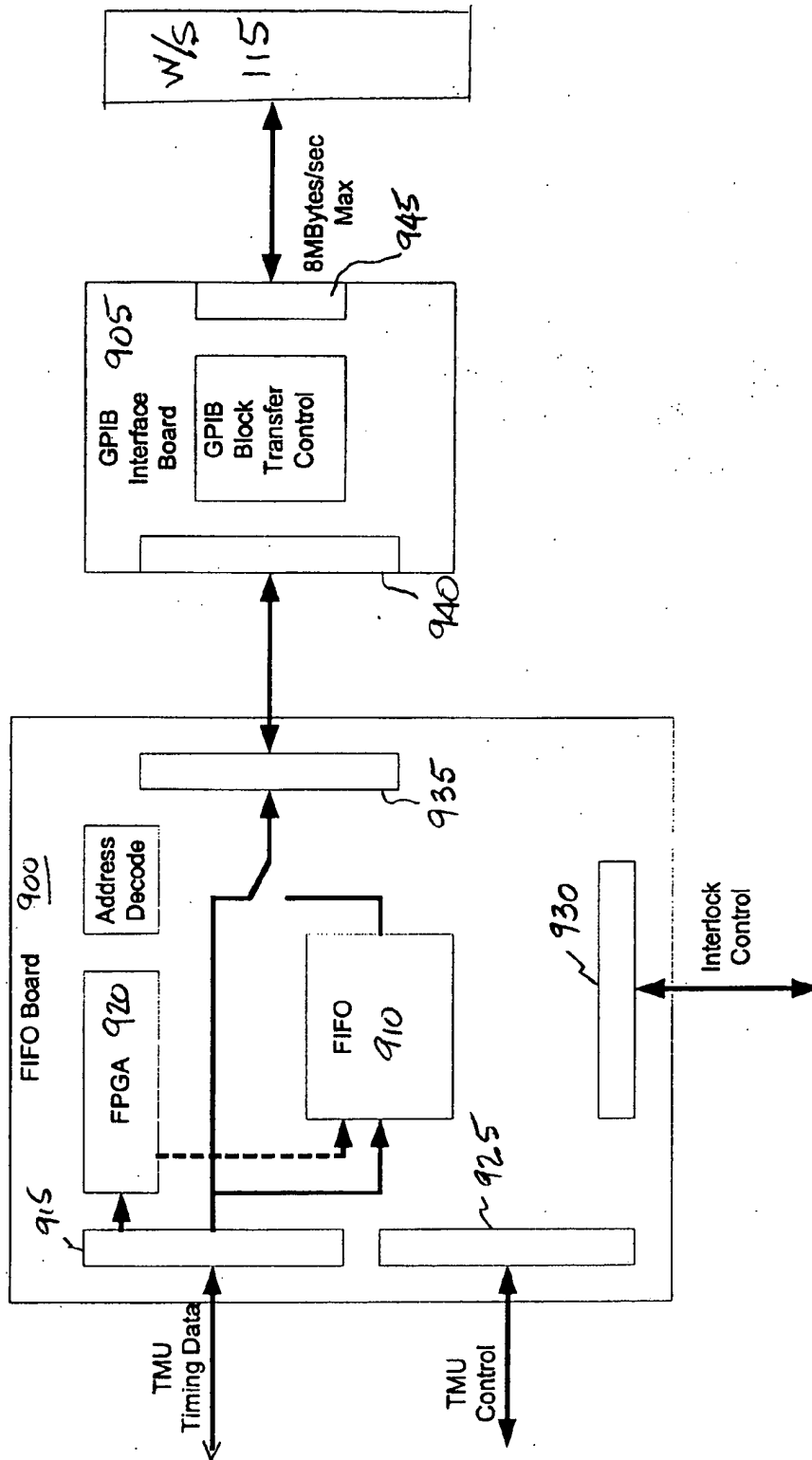


FIG 5

FIG. 7



Timing Subsystem
FIG. 8



Data Path and System Control

FIG. 9

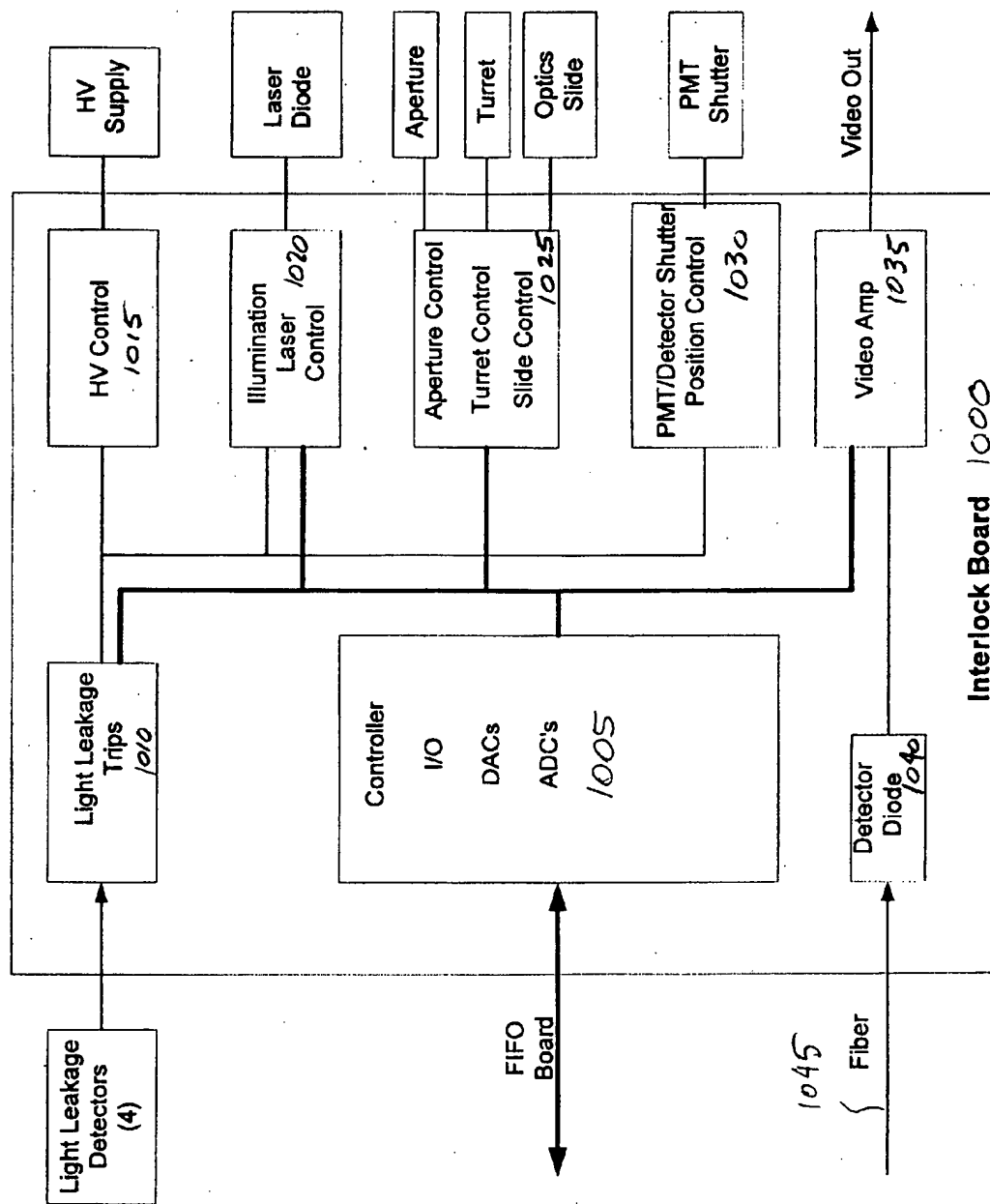
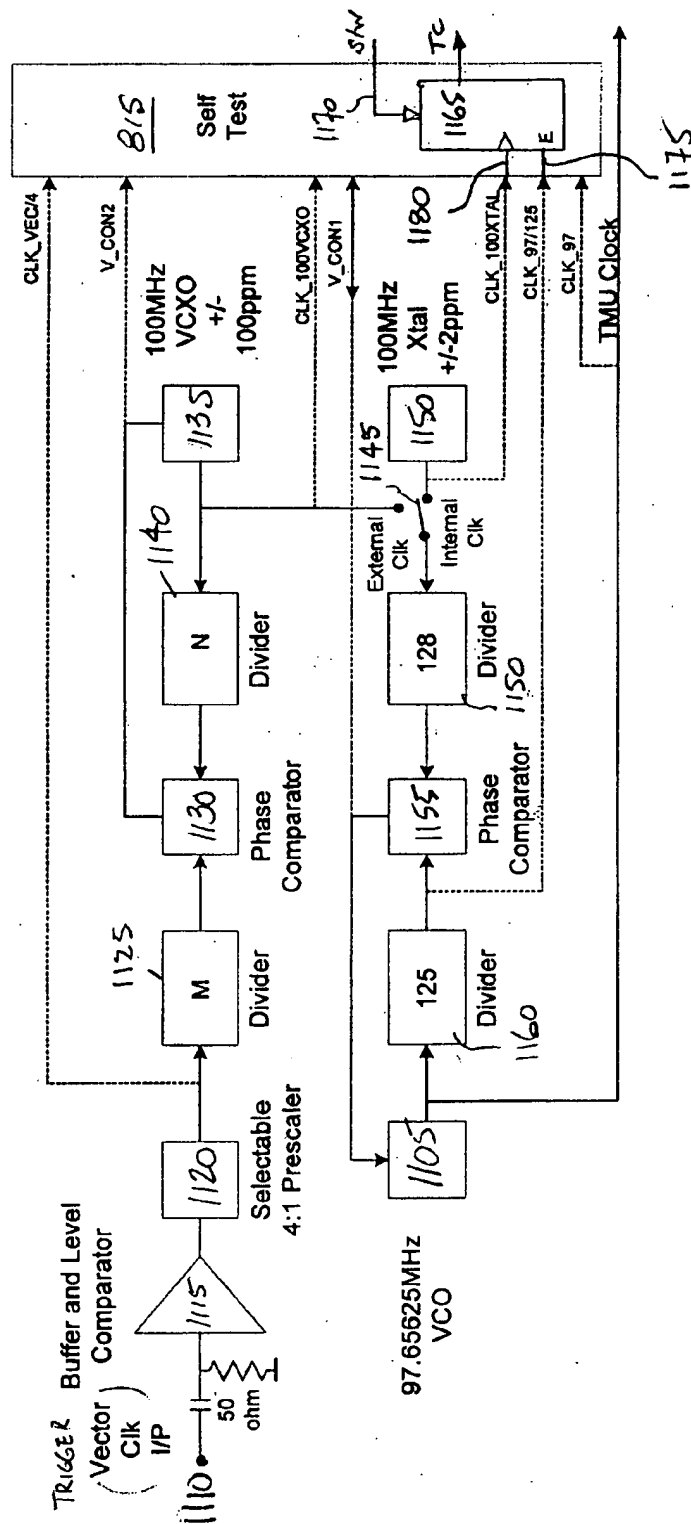


FIG. 10

TMU clock generator.

FIG 11

1100



Interpolator Calibration Method

Counter LSB=1	Counter LSB=0
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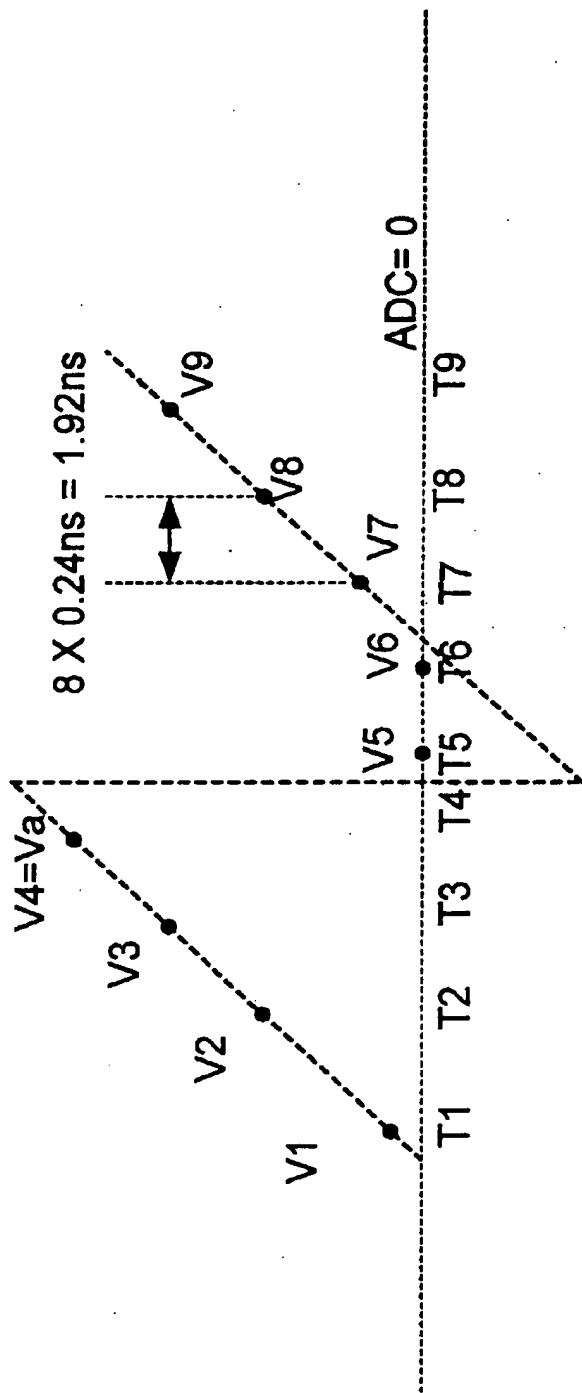


FIG. 12

Interpolator Calibration Method

Counter LSB=1	Counter LSB=0
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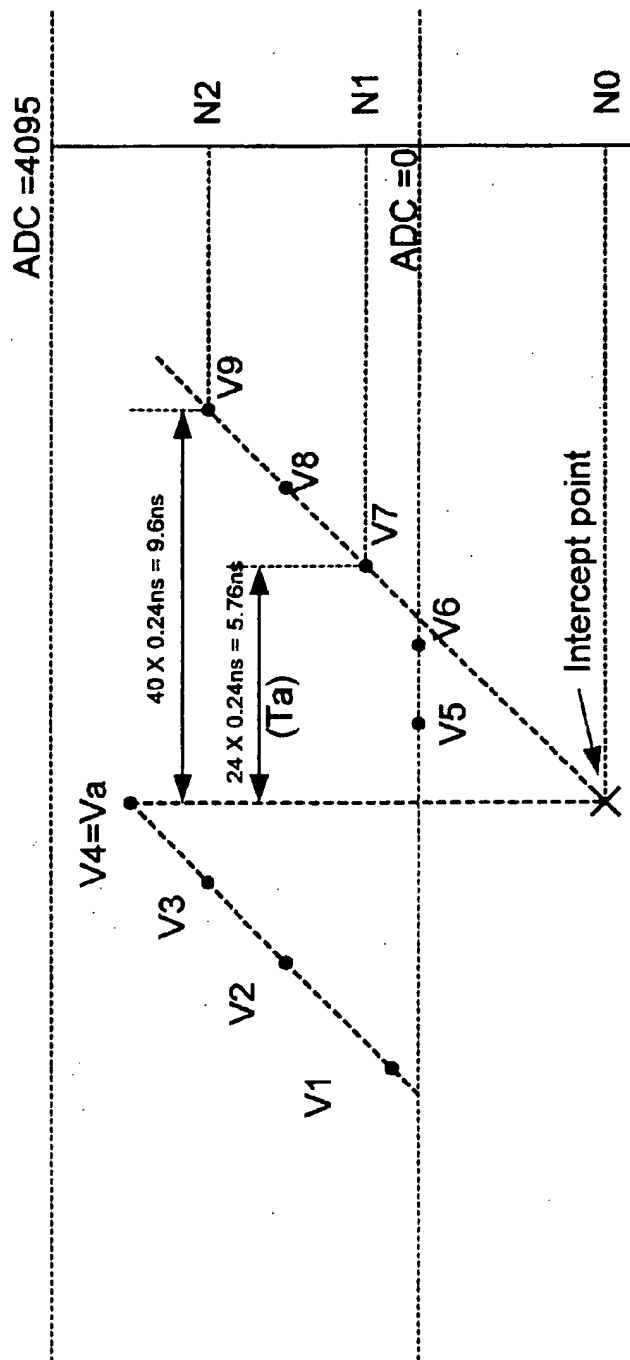


Fig 13

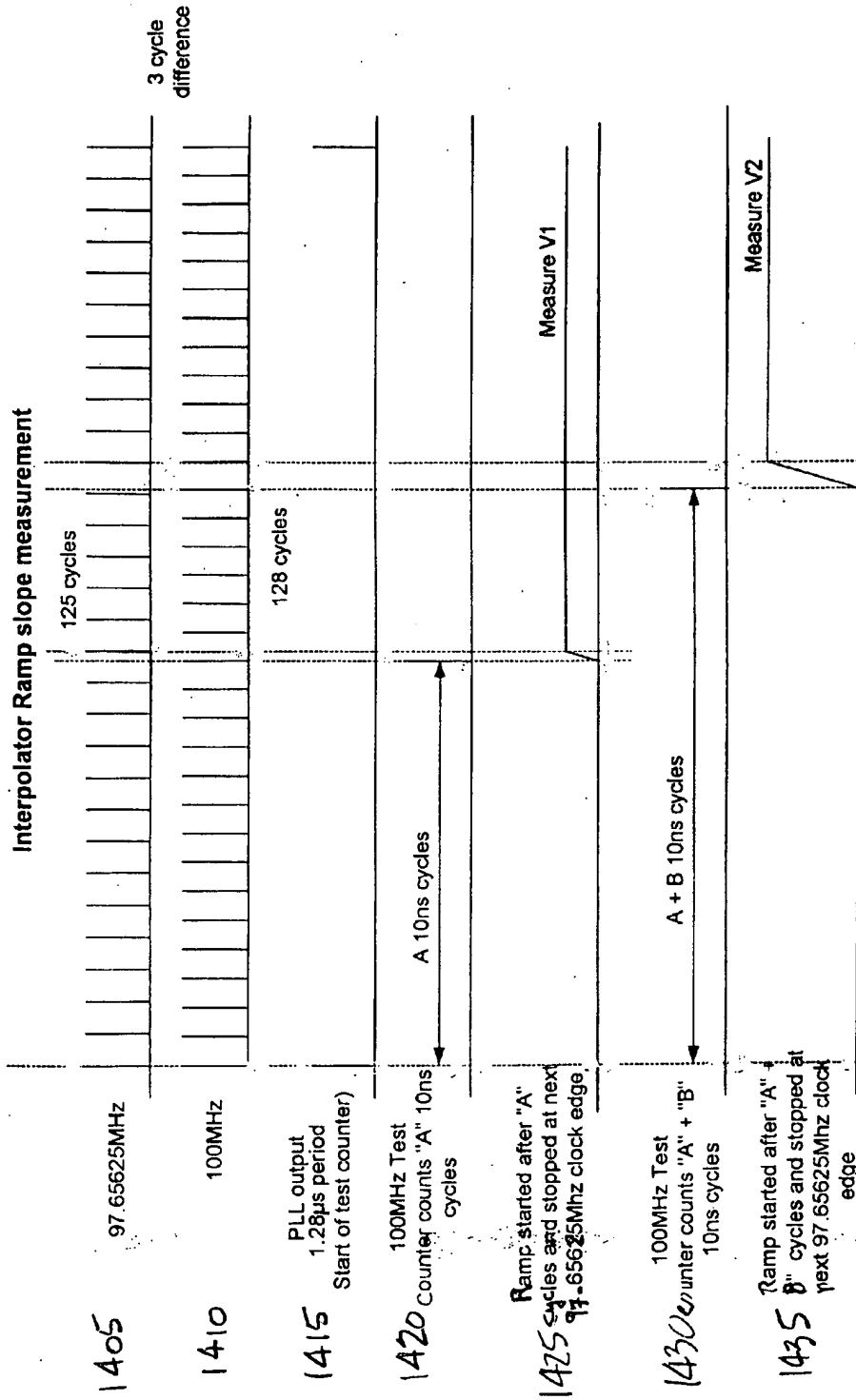


Fig. 14